**What is claimed is:**

1. A multi-stage analog-to-digital ("A/D") converter with pipeline structure comprising:

a sample-and-hold unit for receiving, sampling and holding analog input signals;

a converter section having a plurality of stages for receiving an output of the sample-and-hold unit and generating digital data with a predetermined number of bits; and

a correction circuit for correcting an offset error by overlapping a least significant bit ("LSB") of data from a previous stage with a most significant bit ("MSB") of data from a subsequent stage when an offset error is caused in the previous stage, receiving the digital data from each stage of the converter section, and outputting digital output data,

wherein a second stage of the converter section has an error correction bit in the digital data thereof for correcting an error caused in a first stage but a third and other stages coming after the third stage do not have an error correction bit.

2. The A/D converter according to Claim 1, wherein each stage of the converter section comprises:

a flash converter for receiving the analog output signals of the sample-and-hold unit and generating digital signals corresponding to the received analog signals; and

a multiplying digital-to-analog converter ("MDAC") for receiving the digiital signals from the flash converter, converting the received digital signals to analog

signals, acquiring a difference between the output of the sample-and-hold unit and the converted analog signals, making a residue signal using the difference, and amplifying the residue signal.

3. The A/D converter according to Claim 2, wherein the converter section comprises a first stage having a flash converter with 5 bits and an MDAC with 5 bits, a second stage having a flash converter with 4 bits and an MDAC with 4 bits, a third stage having a flash converter with 3 bits and an MDAC with 3 bits, and a fourth stage having a flash converter with 3 bits, and wherein the second stage has the error correction bit for correcing the error caused in the first stage and 14 bits of digital output data are generated from the A/D converter.

4. The A/D converter according to Claim 3, wherein gains of the MDAC of the first and the second stage are 16, respectively, and a gain of the MDAC of the third stage is 8.

5. An analog-to-digital ("A/D") converter comprising:

a converter portion having at least three pipelined stages for receiving an analog input and generating a digital output; and

an error correction portion in signal communication with the second of the at least three stages for correcting an error caused in the first of the at least three stages by updating an error correction bit.

6. An A/D converter as defined in Claim 5, further comprising:

sample-and-hold means for receiving, sampling and holding analog input signals;

multi-stage conversion means for receiving an analog output of the sample-and-hold means and generating digital data with a predetermined number of bits wherein a single stage of the conversion means has an error correction bit in the digital data thereof for correcting an error caused in a prior stage; and

correction means for correcting an offset error by overlapping a least significant bit ("LSB") of data from a previous stage with a most significant bit ("MSB") of data from a subsequent stage when an offset error exists in the previous stage, receiving the digital data from each stage of the converter section, and outputting digital results.

7. An A/D converter as defined in Claim 5 wherein each stage of the multi-stage conversion means comprises:

flashing means for receiving analog output signals from the sample-and-hold means and generating digital signals corresponding to the received analog signals; and

multiplying means for receiving the digiital signals from the flashing means, converting the received digital signals to analog signals, acquiring a difference between the output of the sample-and-hold means and the converted analog signals, making a residue signal using the difference, and amplifying the residue signal.

8. An A/D converter as defined in Claim 7 wherein the multi-stage conversion means comprises a first stage having a flash converter with 5 bits and a multiplying

digital-to-analog converter ("MDAC") with 5 bits, a second stage having a flash converter with 4 bits and an MDAC with 4 bits, a third stage having a flash converter with 3 bits and an MDAC with 3 bits, and a fourth stage having a flash converter with 3 bits, and wherein the second stage has the error correction means for correcting the error caused in only the first stage in accordance with an error correction bit.

9. An A/D converter as defined in Claim 8 wherein the MDACs of the first and second stages each provide gains of 16, respectively, and the MDAC of the third stage provides a gain of 8.

10. An A/D converter as defined in Claim 6 wherein the single stage having the error correction bit provides a gain at least twice as great as the gains provided by each subsequent stage of the multi-stage conversion means.

11. A coding method of a multi-stage analog-to-digital ("A/D") converter with pipeline structure comprising (a) a sample-and-hold unit for receiving, sampling and holding analog input signals, (b) a converter section having a plurality of stages for receiving an output of the sample-and-hold unit and generating digital data with a predetermined number of bits, and (c) a correction circuit for correcting an offset error by overlapping a least significant bit ("LSB") of data of a previous stage and a most significant bit ("MSB") of data of a subsequent stage when an offset error is caused in the previous stage, receiving the digital data from each stage of the converter section, and outputting digital output data, wherein a second stage of the converter section has

an error correction bit in the digital data thereof for correcting an error caused in a first stage but a third and other stages coming after the third stage do not have an error correction bit.

12. A method of converting an analog input signal into a digital output signal, the method comprising:

receiving an analog input signal; and

providing at least one subsequent stage of a multi-stage pipelined structure for converting a portion of the received analog signal into a plurality of digital bits without an error bit.

13. A method as defined in Claim 12, further comprising:

sampling and holding the received analog input signal;

receiving the sampled and held signal and generating corresponding digital data having a predetermined number of bits;

correcting an offset error by overlapping a least significant bit ("LSB") of data from a previous stage with a most significant bit ("MSB") of data from a subsequent stage when an offset error is caused in the previous stage.

14. A method as defined in Claim 12, further comprising:

receiving digital data from each stage of the multi-stage pipelined structure, and outputting combined digital output data including all bits from all stages with the single

exception of an error correction bit from a subsequent but non-final stage for correcting an error caused in a previous stage.

15. A method as defined in Claim 13, further comprising:

receiving the sampled and held analog signals and generating digital signals corresponding to the received analog signals; and

converting the generated digital signals into analog signals, acquiring a difference between the original sampled and held analog signals and the converted analog signals, making a residue signal using the difference, and amplifying the residue signal.

16. A method as defined in Claim 12, further comprising:

converting the least significant portion of the analog signal into 5 bits at a first stage;

converting the next more significant portion of the analog signal into 3 bits plus an error correction bit at a second stage;

converting the next more significant portion of the analog signal into 3 bits at a third stage; and

converting the most significant portion of the analog signal into 3 bits at a fourth stage to generate 14 bits of digital output data.

17. A method as defined in Claim 16, further comprising:

providing gains at the first and the second stages of 16, respectively, and a gain of at the third stage of 8.

18. A method as defined in Claim 13, further comprising:

receiving the sampled and held analog signal and generating digital data with a predetermined number of bits wherein a single stage of a multi-staged pipelined structure supports an error correction bit in the digital data thereof for correcting an error caused in a prior stage; and

correcting an offset error by overlapping a least significant bit ("LSB") of data from a previous stage with a most significant bit ("MSB") of data from a subsequent stage when an offset error exists in the previous stage, receiving the digital data from each stage of the converter section, and outputting combined digital results.

19. A method as defined in Claim 13, further comprising:

flashing the sampled and held analog signal and generating a digital signal corresponding to the flashed analog signal; and

converting the generated digital signal into an analog signal, acquiring a difference between the output of the sampled and held analog signal and the converted analog signal, making a residue signal using the difference, and amplifying the residue signal.

20. A method as defined in Claim 13, further comprising:

providing a gain at a stage that supports an error correction bit of at least twice as great as the gain provided by each subsequent stage of a multi-stage pipelined structure.